(12) UK Patent Application (19) GB (11) 2 187 054 (13) A

(43) Application published 26 Aug 1987

(21) Application No 8604342

(22) Date of filing 21 Feb 1986

(71) Applicant
STC plc,
(Incorporated in United Kingdom),
190 Strand, London WC2R 1DU

(72) Inventor
Stephen John Harrold

(74) Agent and/or Address for Service
J.P.W. Ryan, STC Patents, Edinburgh Way, Harlow, Essex CM20 2SH

(51) INT CL[4]
H03M 1/36

(52) Domestic classification (Edition I)
H3H 14A 14D 3C 3D 6A 6B 6D 6E 7B 7F 8B AB
U1S 2123 2202 H3H

(56) Documents cited

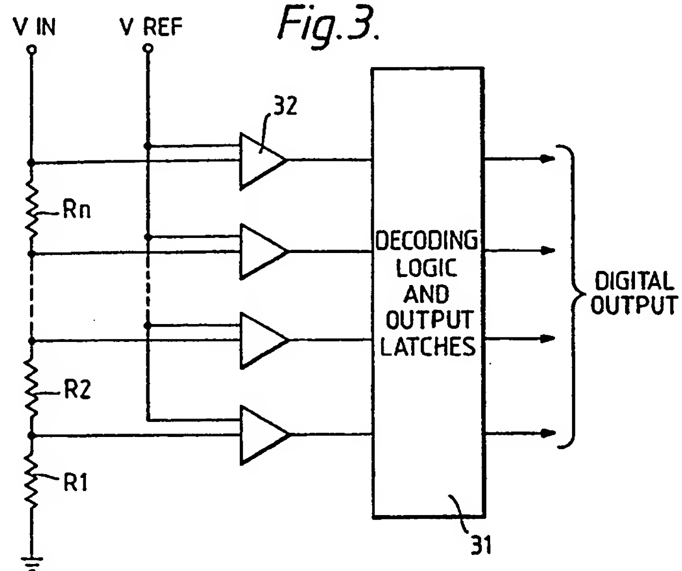
GB A 2021346	GB 1261003
GB 1568101	GB 1240686
GB 1524527	GB 1216081
GB 1391131	GB 1113431

(58) Field of search
H3H
Selected US specifications from IPC sub-classes H03K H03M

(54) Analogue to digital converters

(57) An analogue to digital converter comprises a plurality of amplifiers (32) whose inputs are fed with an analogue signal via a resistor chain (R1 to Rn). The amplifier outputs are coupled to a decoding logic and output latch circuit (31) which generates a digital output corresponding to the analogue input. The arrangement reduces the effects of sampling-skew and can thus operate at high frequencies.

Fig.3.



The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

GB 2 187 054 A

Fig. 1.

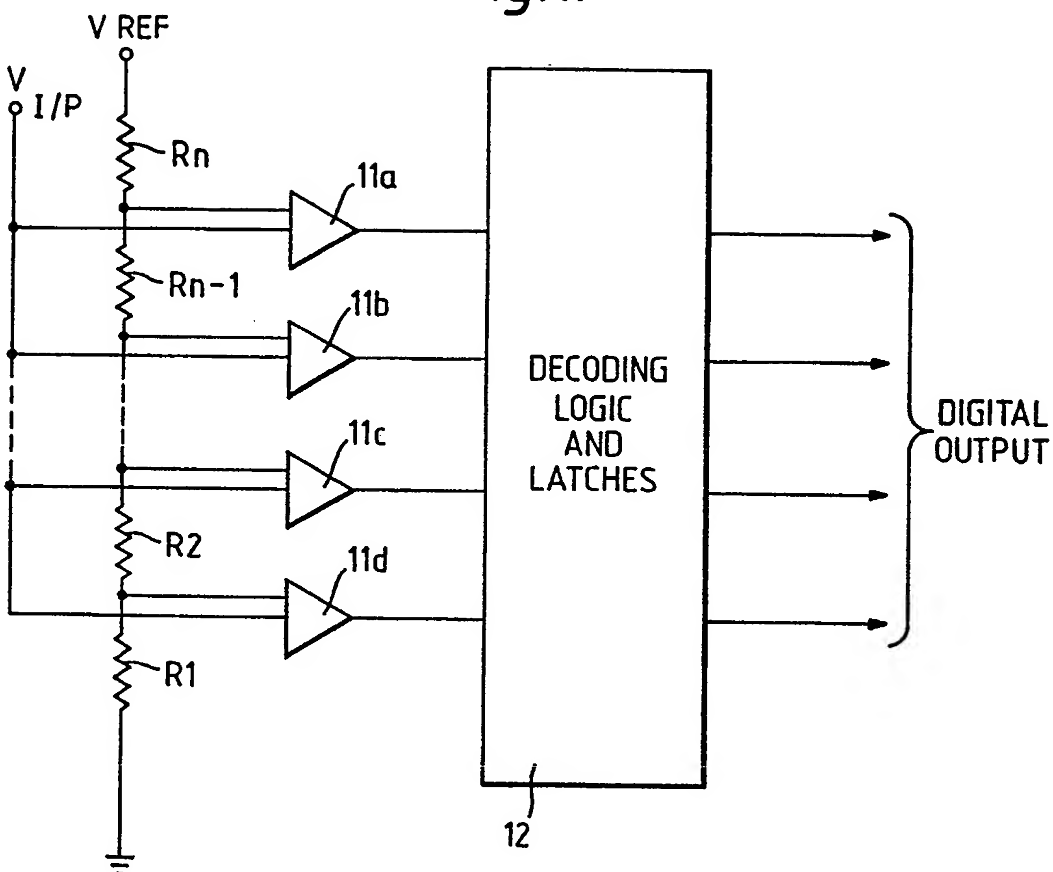

V REF
V I/P
Rn
Rn-1
R2
R1
11a
11b
11c
11d
DECODING LOGIC AND LATCHES
12
DIGITAL OUTPUT

Fig.2.

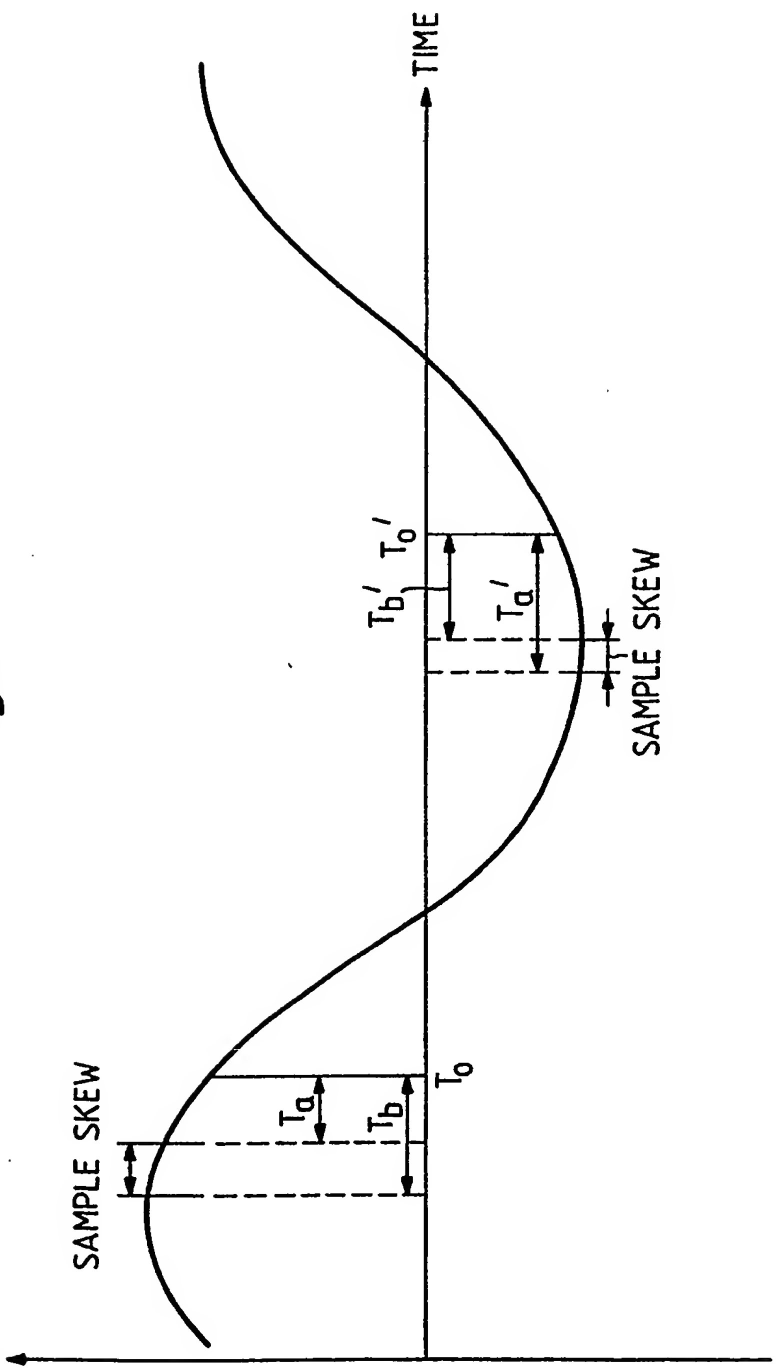


Fig.3.

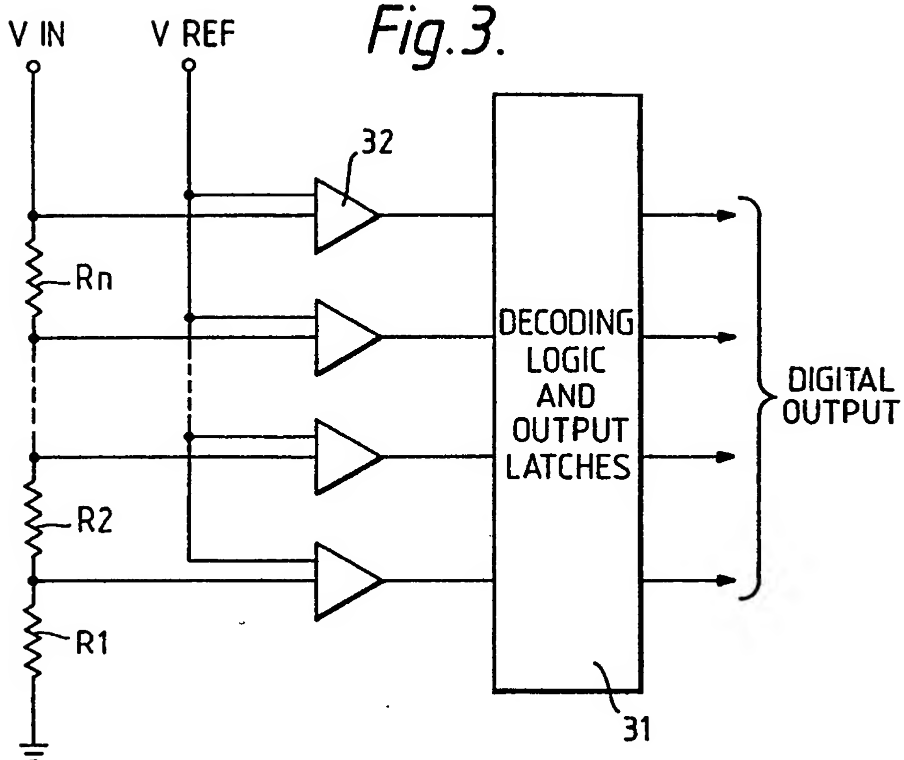
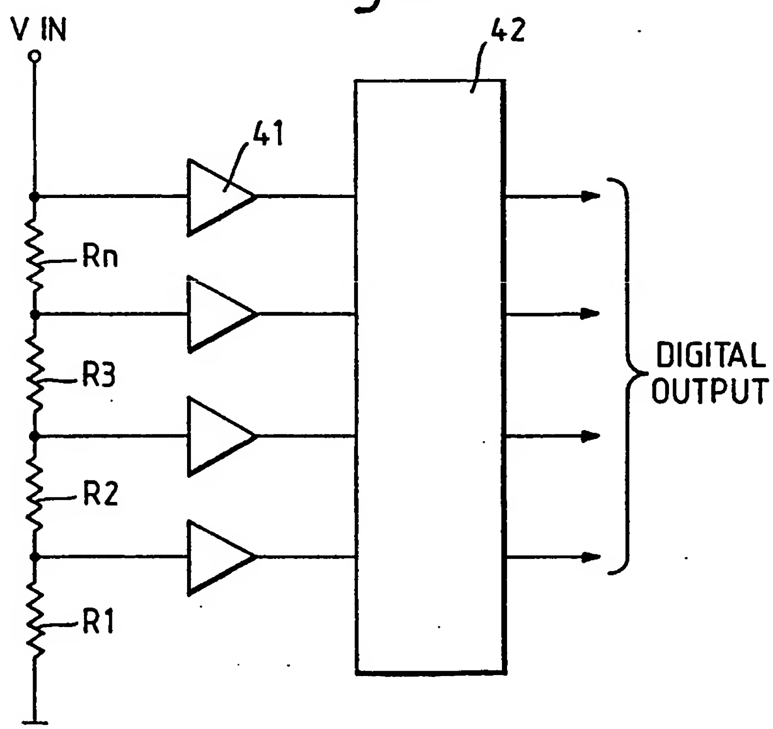

V IN
V REF
32
Rn
R2
R1
DECODING LOGIC AND OUTPUT LATCHES
31
DIGITAL OUTPUT

Fig.4.


V IN
42
41
Rn
R3
R2
R1
DIGITAL OUTPUT

SPECIFICATION

Analogue to digital converters

This invention relates to analogue to digital converters and in particular to an architecture for high speed converters. Conventional high-speed ('flash') analogue-to-digital converters (ADCs) are generally organised with the architecture illustrated in Figure 1 of the accompanying drawings. In this construction a parallel row of comparators (11) is fed with the input (analogue) signal V_{in}, and each comparator compares this input with a reference signal derived from a reference voltage V_{ref} via a resistor chain R1 to Rn.- Each comparator 11 which has a reference signal less than the input signal at the sampling time will have an output in one state (either 'high' or 'low'), while the other comparators with a reference signal greater than the input signal will have an output in the opposite state. The output of the row of comparators is thus comparable to a thermometer scale, with the magnitude of the input signal at the sampling time indicated by the position of the change in comparator output from one state to another. A decoding logic and output latch circuit 12 can then convert this thermometer scale output into any required digital format (e.g. magnitude-only or two's complement).

Limitations to the speed at which this architecture can operate come from two main areas. Firstly, the speed at which the latches can be clocked is limited, and secondly the propagation delay from the input through to the outputs may vary, depending upon which path is followed, and this will cause errors in the digital output if the input signal bandwidth is too high. Figure 2 of the accompanying drawings illustrates the operation of the circuit of Figure 1. Referring to Figure 2, a clock edge triggering the output latches at time T_o is effectively sampling the state of the input signal V, e.g. of comparator 11a, some time T_a earlier, where T_a is the propagation delay between the input and that output. This delay is not constant but will vary according to the signal condition at the comparator input. Similarly a delay T_b is exhibited by comparator 11b and so on. As the propagation delay varies with the signal path examined, then each output latch will be effectively sampling the input signal at a different time, and thus at diferent states. Thus, at the next sampling time, delays T_a and T_b different from T_a and T_b are experienced. To make matters worse the relative magnitudes of the delay times may be reversed. This spread of sampling times or sampling-skew, sometimes referred to as the 'aperture uncertainty', can be ignored if the spread in the values of the input signal being sampled is small compared to the resolution of the ADC concerned. However, in practice this is difficult to insure, and limits the maximum frequency of the input signal can be sampled.

The object of the present invention is to minimise or to overcome this disadvantage.

According to the invention there is provided an analogue to digital converter, including a plurality of input amplifiers, a resistor chain each node of which is coupled to an amplifier input and via which, in use, an input analogue signal is fed to the amplifier, and a decoding circuit coupled to the amplifier outputs whereby a digital signal corresponding to the input analogue signal is generated.

One of the chief causes of sampling-skew in a conventional analogue to digital converter is the delay variation in the comparators. Each comparator receives a different reference signal and is thus under different bias conditions. Thus each comparator is subject to a different propagation delay. We have found that this disadvantage of conventional converters may be overcome by providing a common reference signal thus providing uniform bias conditions.

Embodiments of the invention will now be described with reference to Figures 3 and 4 of the accompanying drawings, in which:-

Figure 3 is a schematic circuit diagram of a high speed analogue to digital converter; and

Figure 4 shows an alternative converter construction.

Referring to Figure 3, the converter includes a decoding logic and output latch circuit 31 having a plurality of inputs to each of which a two-input amplifier or comparator 32 is coupled.

One input of each comparator 32 is directly coupled to a reference voltage source V_{ref}. An analog input signal V_{in} is fed to the other inputs of the comparators 32 via a resistor chain R1 to Rn, the comparator inputs being connected one to each node of the chain. The comparator outputs are coupled to the decoding logic and output latch circuit 31 which circuit generates a digital output corresponding to the analogue input. The relative values of the resistors R11 to R14 are chosen such that a linear A/D converter is provided. Although four comparators are chosen it will be appreciated that the technique is not so limited.

As the comparators 32 will receive the same reference signal there is no variation in propogation delay. Slight aperture uncertainty will of course arise from the delay of the input signal as it passes along the resistor chain which is loaded by the input capacitance of each comparator. This effect can be rendered insignificant to using small value resistors. Further, a buffer input stage (not shown), e.g. a source or emitter follower, may be provided at the input of each amplifier to reduce the input capacitance of the converter.

The values of the resistors R1 to Rn are preferably such that a linear conversion is provided. Each resistor value may be calculated from the following formula:-

$$R_n = -V_R \; R_T \left[\frac{1}{V_m\left(\frac{N-n}{N}\right)-V_R} - \frac{1}{V_n\left(\frac{N-n+1}{N}\right)-V_R} \right]$$

$$2 \leq n \leq N$$

and

$$R_1 = R_T - \sum_{i=2}^{N} R_i = -V_R \; R_T \left[\frac{1}{V_m\left(\frac{N-1}{N}\right)-V_R} \right]$$

wherein

V_R is the reference voltage

R_T is the total input impedance

V_m is the maximum input voltage

N is the number of quantization levels.

Thus, in a typical example where a 4 bit converter having 16 quantization levels and an input impedance of 50 ohms is required, the following resistor values have been calculated using the above formula. A reference voltage V_R of -1 volt and an input voltage in the range 0 to +1 volts were assumed.

R_1=25.806ohm	R_5=1.085ohm	R_9 = 1.449ohm	R_{13}=2.105ohm
R_2= 0.860 ohm	R_6=1.140ohm	R_{10}=1.581ohm	R_{14}=2.339ohm
R_3= 0.920ohm	R_7=1.231ohm	R_{11}=1.732ohm	R_{15}=2.614ohm
R_4 = 0.985ohm	R_8=1.333ohm	R_{12}=1.905ohm	R_{16}=2.941ohm

Further, a buffer input stage (not shown), e.g. a source or emitter follower, may be provided at the input of each amplifier to reduce the input capacitance of the converter.

An alternative construction is shown in Figure 4. As a common reference signal is employed it is not essential to use two-input comparators. Figure 4 shows a converter in which an input signal is fed via a resistor chain R1 - Rn to a plurality of single input amplifiers 41. Typically each amplifier 41 comprises standard logic inverter. The outputs of the amplifiers are fed to a decoding logic and output latch circuit 42 which provides a digital signal corresponding to the analogue input.

The analogue to digital converters described herein are intended for use in high capacity data transmission systems, but they are not of course so limited and can be employed in other, e.g. computer, applications.

CLAIMS

1. An analogue to digital converter, including a plurality of input amplifiers, a resistor chain each node of which is coupled to an amplifier input and via which, in use, an input analogue signal is fed to the amplifier, and a decoding circuit coupled to the amplifier outputs whereby a digital signal corresponding to the input analogue signal is generated.

2. An analogue to digital converter as claimed in claim 1, wherein the relative values of the resistors of said chain are such that a linear conversion is provided.

3. An analogue to digital converter as claimed in claim 1 or 2, wherein a buffer stage is provided at the input of each said amplifier whereby the input capacitance of that amplifier is reduced.

4. An analogue to digital converter as claimed in claim 1, 2 or 3, wherein said amplifiers are logic inverters.

5. An analogue to digital convertor as claimed in claim 1, 2 or 3, wherein said amplifiers are two-input comparators.

6. An analogue to digital converter substantially as described herein with reference to and as shown in Figure 3 or Figure 4 of the accompanying drawings.

7. A data transmission system incorporating analogue to digital converters as claimed in any one of claims 1 to 6.

Printed for Her Majesty's Stationery Office by Croydon Printing Company (UK) Ltd, 7/87, D8991685.
Published by The Patent Office, 25 Southampton Buildings, London WC2A 1AY, from which copies may be obtained.